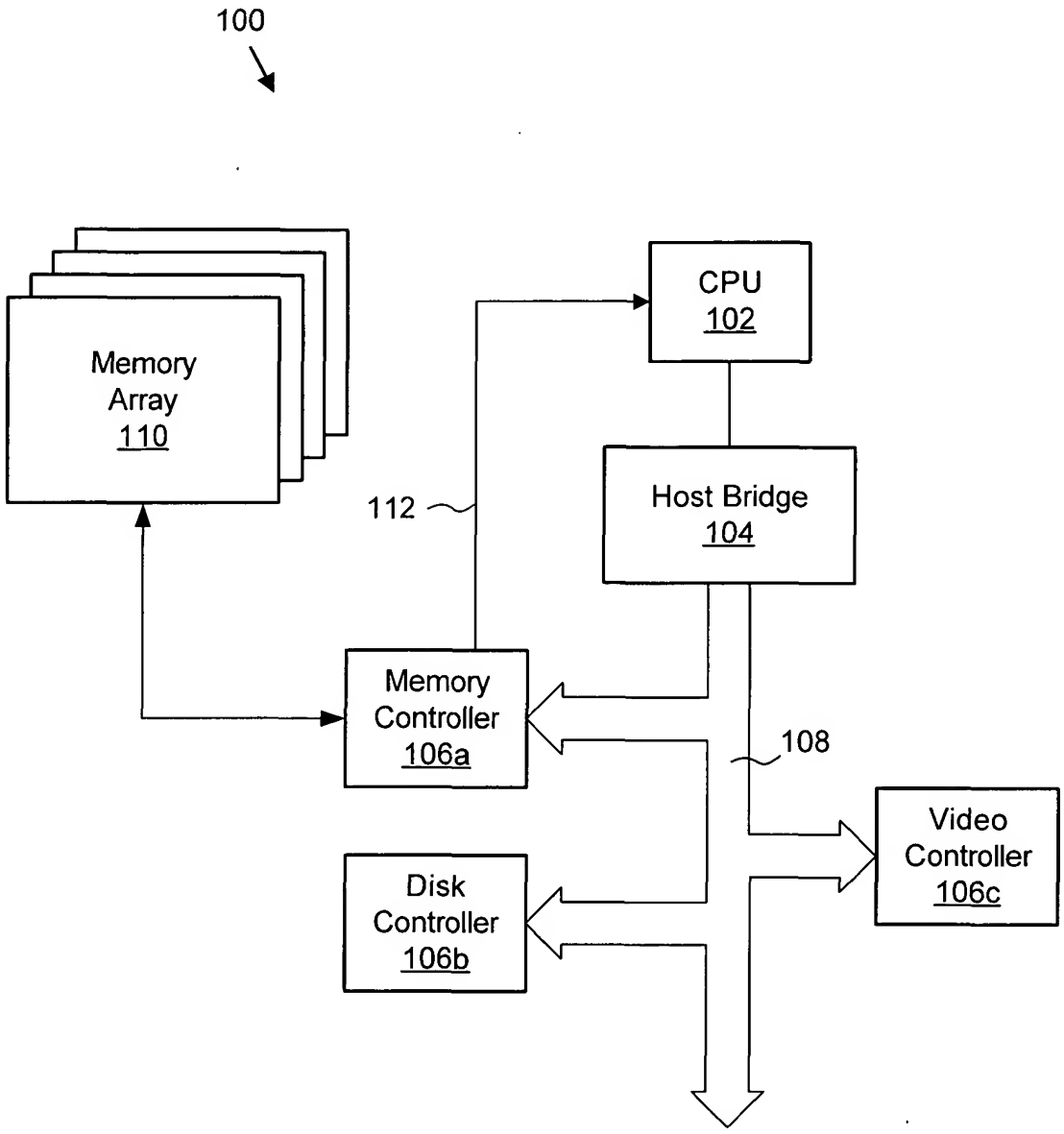
100
Memory Array 110
CPU 102
Host Bridge 104
112
Memory Controller 106a
108
Video Controller 106c
Disk Controller 106b

Fig. 1

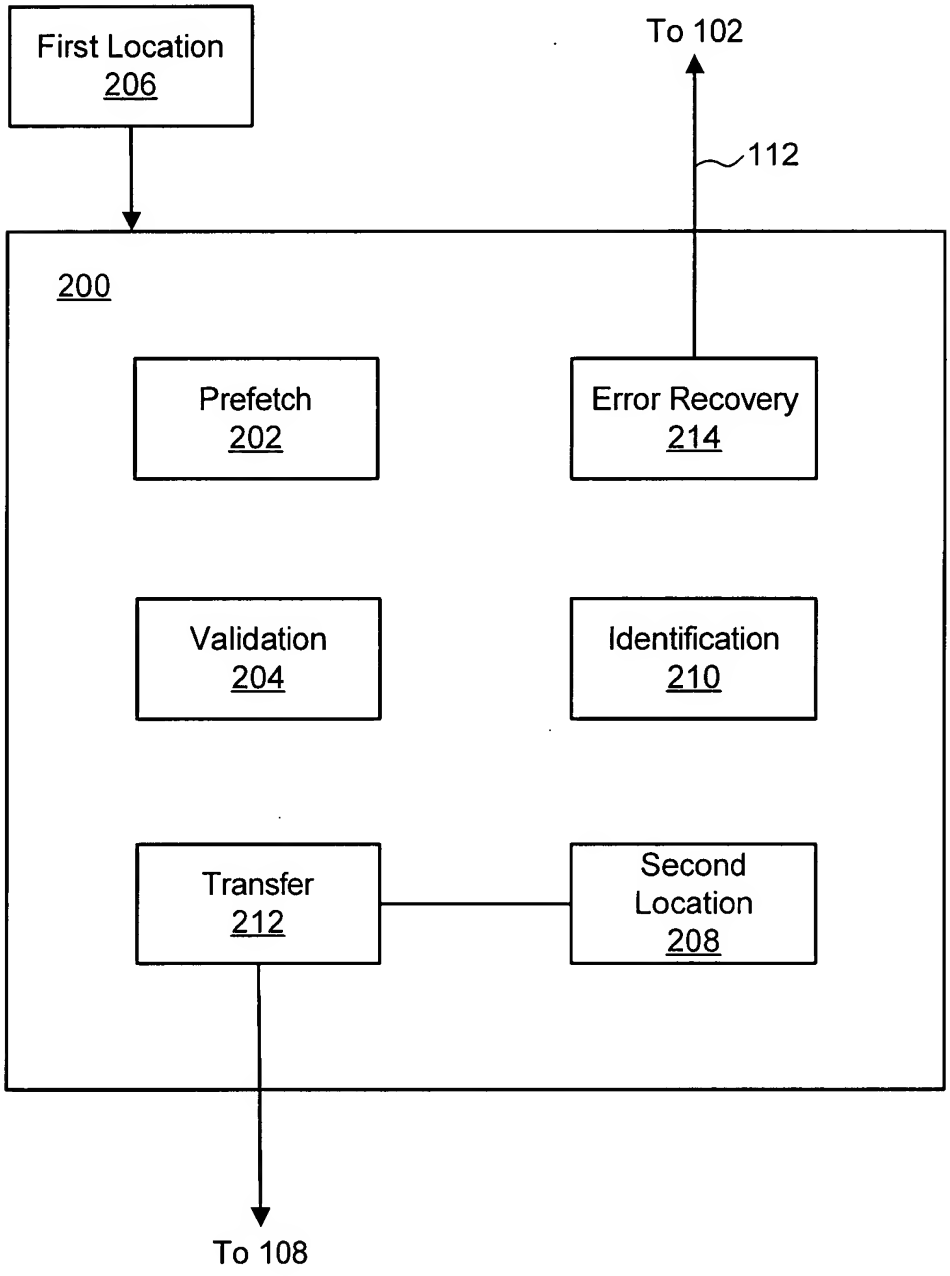
First Location
206
To 102
112
200
Prefetch
202
Error Recovery
214
Validation
204
Identification
210
Transfer
212
Second
Location
208
To 108

Fig. 2

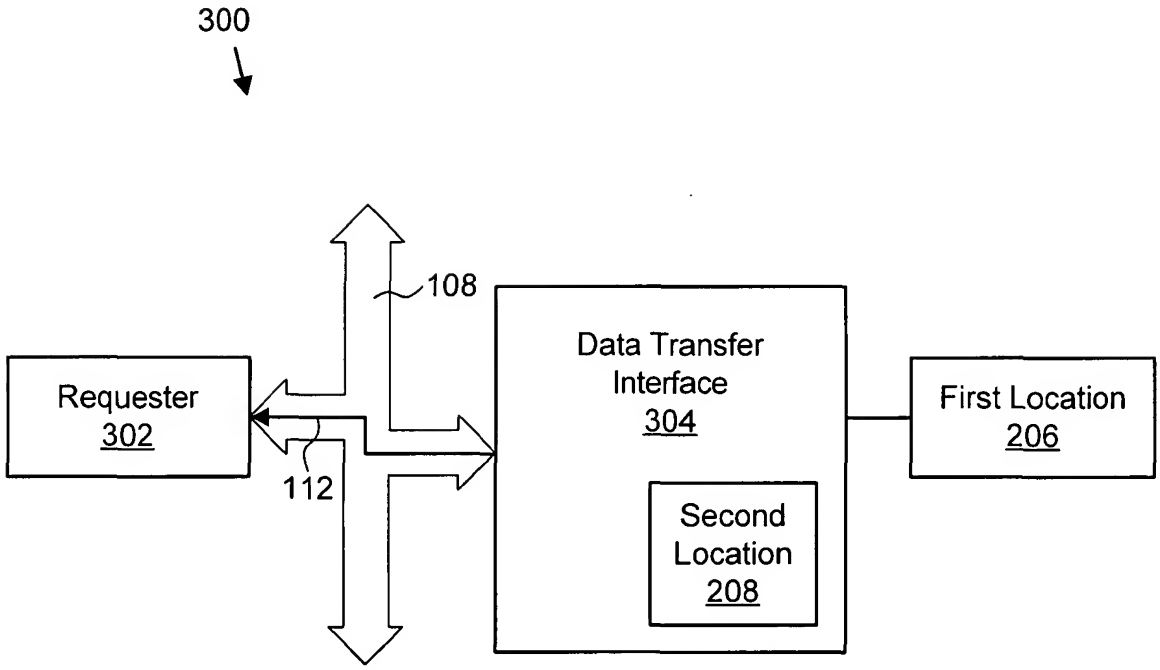
300
108
Requester
302
112
Data Transfer
Interface
304
Second
Location
208
First Location
206

Fig. 3

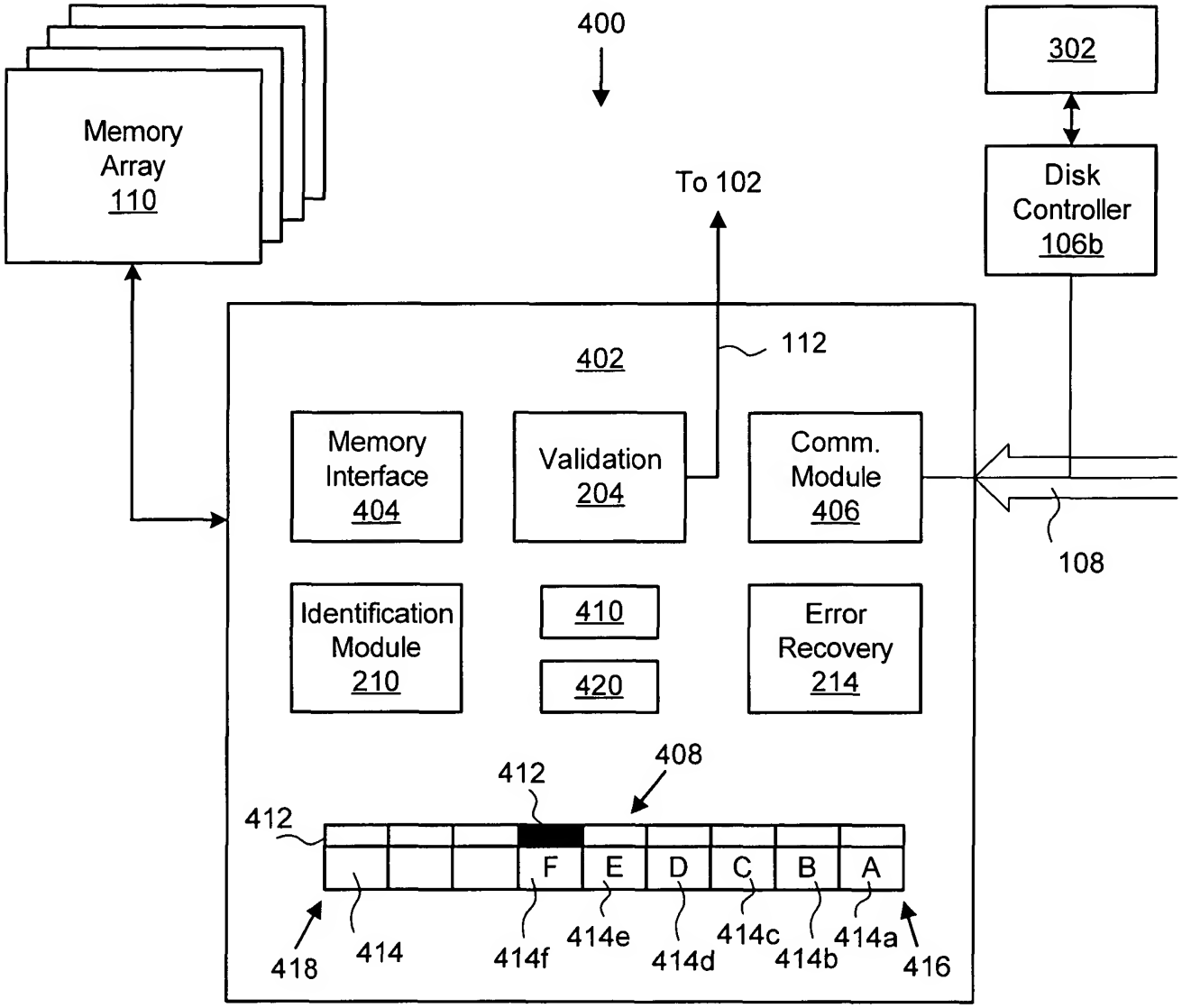
400
302
Memory Array 110
To 102
Disk Controller 106b
112
402
Memory Interface 404
Validation 204
Comm. Module 406
108
Identification Module 210
410
420
Error Recovery 214
408
412
412
F
E
D
C
B
A
418
414
414f
414e
414d
414c
414b
414a
416

Fig. 4

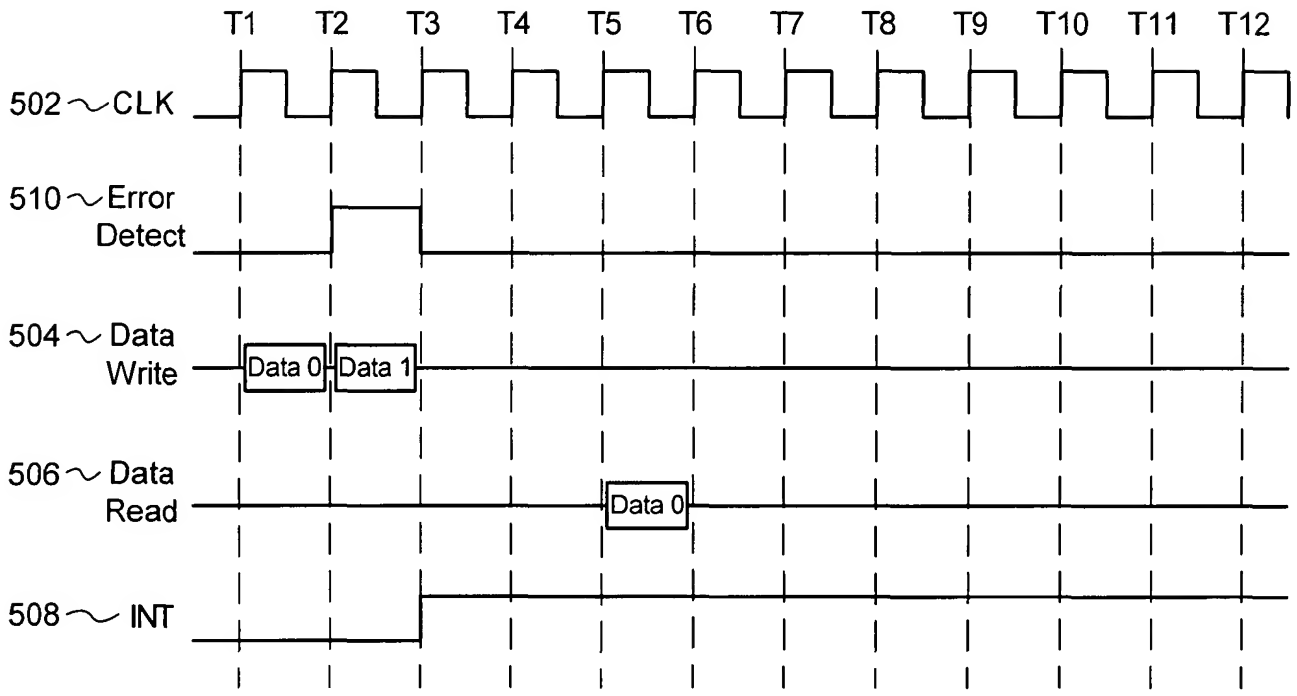
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
502 CLK
510 Error Detect
504 Data Write
Data 0
Data 1
506 Data Read
Data 0
508 INT

Fig. 5

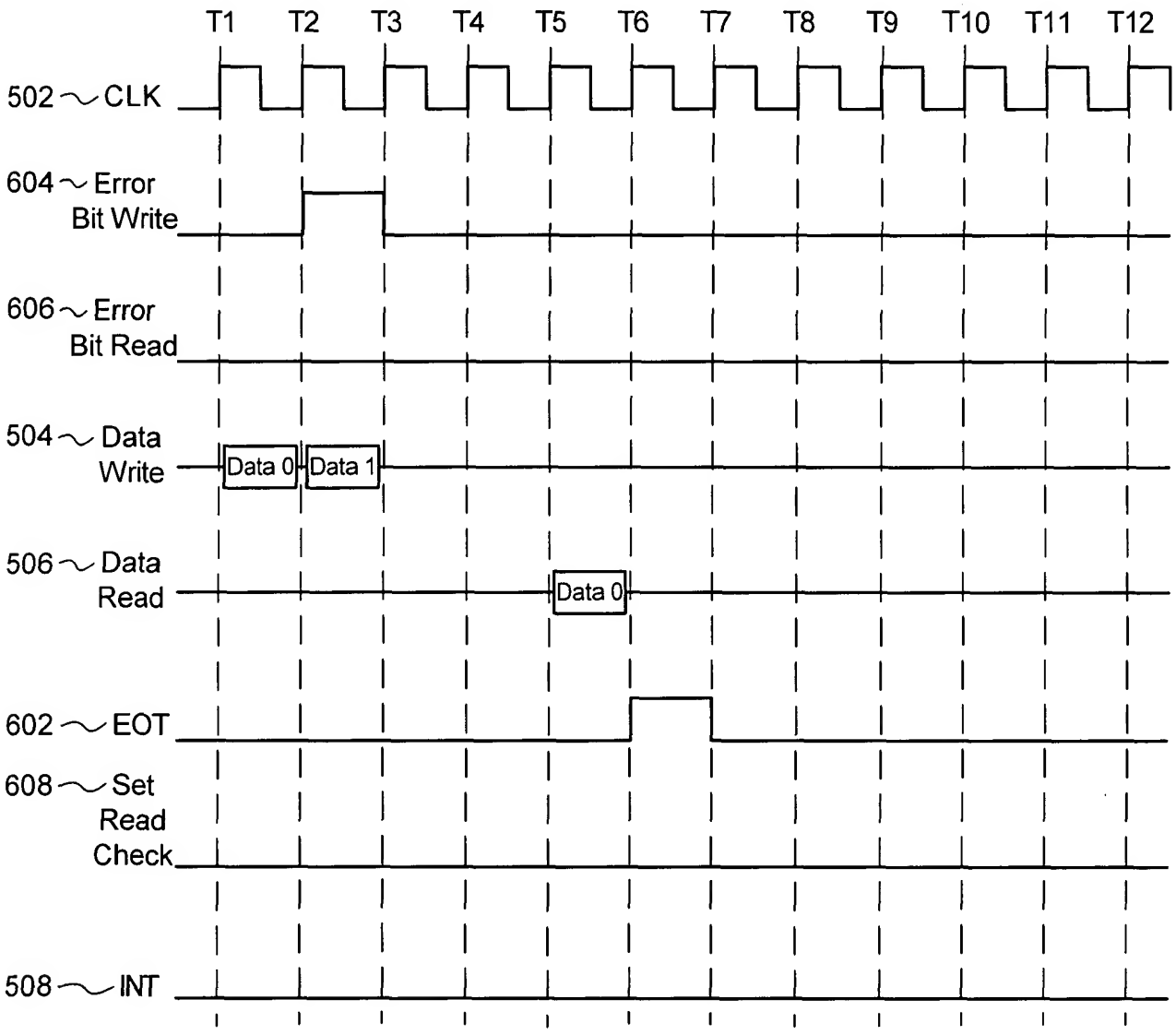
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
502 CLK
604 Error Bit Write
606 Error Bit Read
504 Data Write
Data 0
Data 1
506 Data Read
Data 0
602 EOT
608 Set Read Check
508 INT

Fig. 6

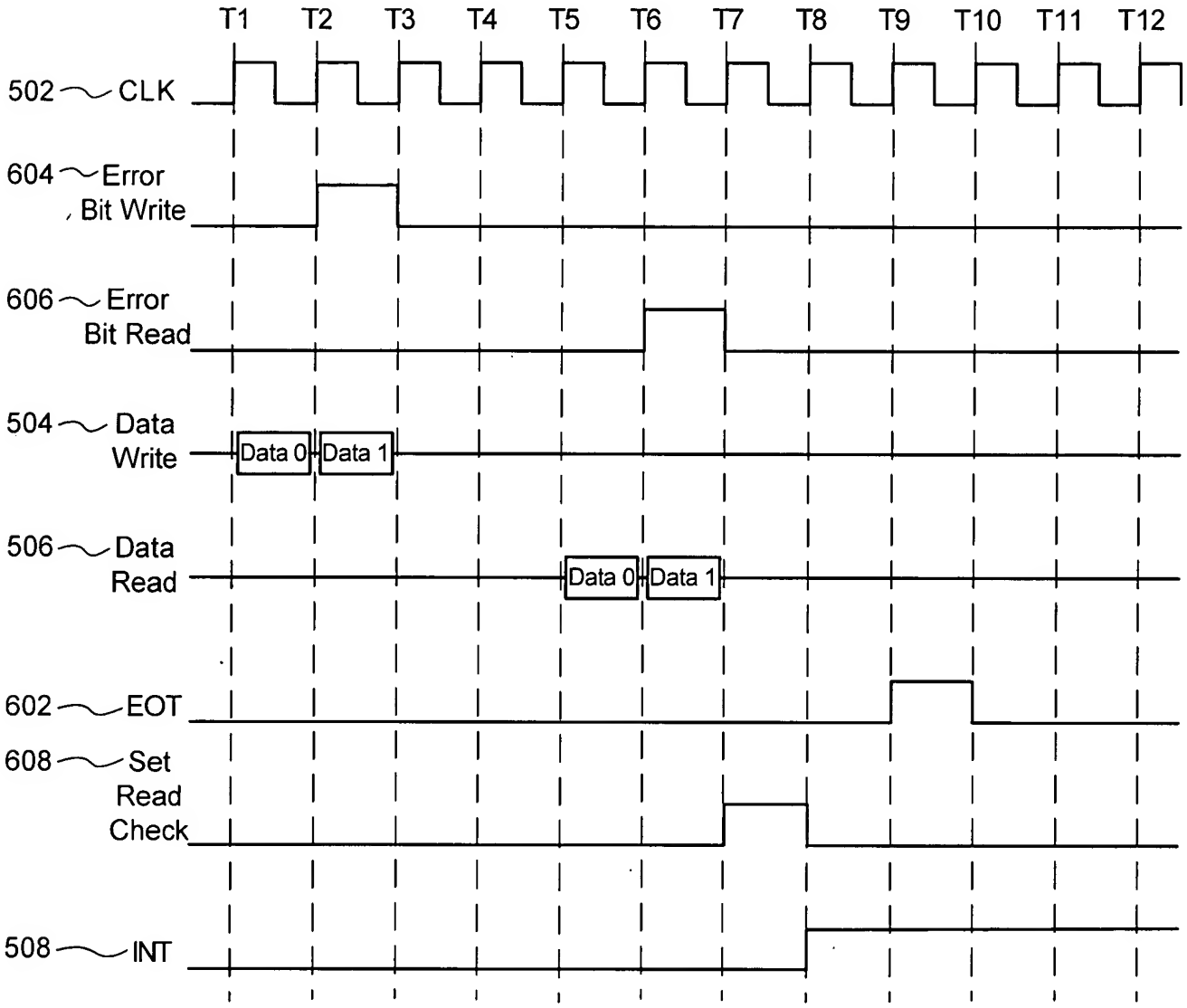
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
502 CLK
604 Error Bit Write
606 Error Bit Read
504 Data Write
Data 0
Data 1
506 Data Read
Data 0
Data 1
602 EOT
608 Set Read Check
508 INT

Fig. 7

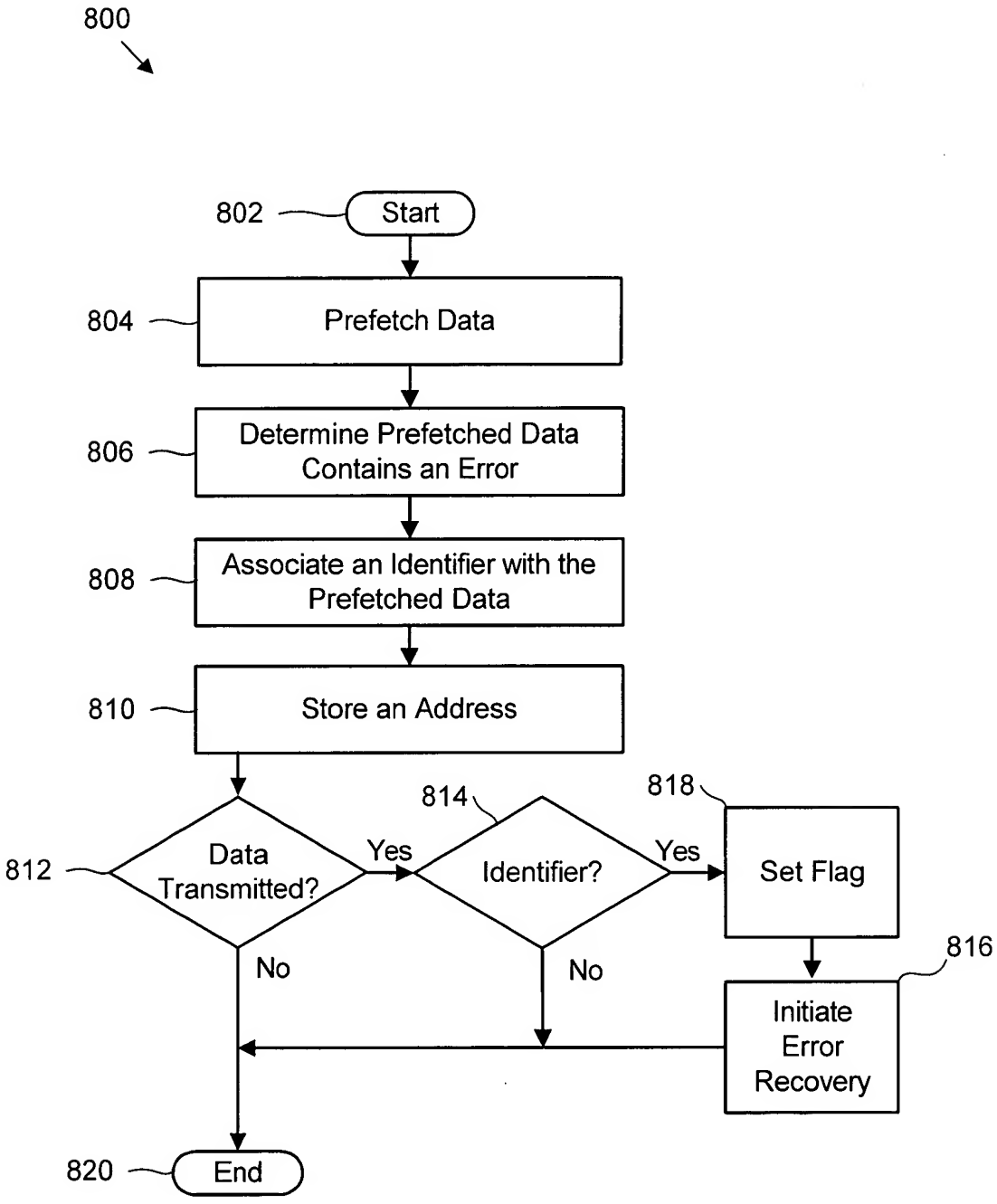
800
802
Start
804
Prefetch Data
806
Determine Prefetched Data Contains an Error
808
Associate an Identifier with the Prefetched Data
810
Store an Address
812
Data Transmitted?
Yes
No
814
Identifier?
Yes
No
818
Set Flag
816
Initiate Error Recovery
820
End

Fig. 8